

**What Is Claimed Is:**

1           1. A semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide  
2 semiconductor (MOS) integrated circuit comprising:

3           a substrate of a first conductivity type forming a base for said semiconductor structure;

4           a first region of a second conductivity type within said substrate for forming a drain of a first  
5 MOS transistor;

6           a second region of the second conductivity type within said substrate for forming a source  
7 of the first MOS transistor;

8           a third region of the second conductivity type within said substrate coupled to a gate of a  
9 second MOS transistor, wherein

10           a fourth region of the first conductivity type is disposed adjacent to the third region of the  
11 second conductivity type for surrounding said first MOS transistor with an additional pick-up  
12 diffusion to reduce a turn-on speed or a longer channel length to increase a drain-base breakdown  
13 voltage of said first MOS transistor.

1           2. The semiconductor structure of claim 1, wherein said fourth region of the first conductivity  
2 type is disposed adjacent to the third region of the second conductivity type for surrounding said first  
3 MOS transistor with an additional pick-up diffusion to reduce a turn-on speed and a longer channel  
4 length to increase a drain-base breakdown voltage of said first MOS transistor.

1           3. The semiconductor structure of claim 1, further comprising:

2           a pre-buffer circuit coupled to said gate of the first MOS transistor; and

3           an output pad coupled to said first region of the first MOS transistor.

1           4. The semiconductor structure of claim 1, further comprising:

2           a first channel region of the second conductivity type having a first channel length and  
3 disposed between said first and second regions of said first MOS transistor;

4           a second channel region of the second conductivity type having a second channel length and  
5 disposed between said first and third regions,

6           wherein said first channel length is greater than said second channel length to further increase  
7 the device breakdown voltage for reducing the turn-on speed of said first MOS transistor.

1           5. A semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide  
2 semiconductor (MOS) integrated circuit comprising:

3           a substrate of a first conductivity type forming a base for said semiconductor structure;

4           a pair of first regions of a second conductivity type within said substrate for defining a first  
5 channel region of the second conductivity type for a first MOS transistor; and

6           a pair of second regions of the second conductivity type within said substrate for defining a  
7 second channel region of the second conductivity type for a second MOS transistor,

8           wherein the channel length of said first channel region is greater than the channel length of  
9 said second channel region to reduce a turn-on speed of said first MOS transistor

1           6. The semiconductor structure of claim 5, further comprising:  
2           a pre-buffer circuit coupled to said first channel region; and  
3           an output pad coupled to one of said pair of first regions of said second conductivity type and  
4           one of said pair of second regions of said second conductivity type.

1           7. The semiconductor structure of claim 5, further comprising a third region of the first  
2           conductivity type adjacent to one of said second regions of said second conductivity type for  
3           surrounding said MOS transistor with an additional pick-up diffusion to further restrain the turn-on  
4           of said first MOS transistor

1           8. A semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide  
2           semiconductor (MOS) integrated circuit comprising:

3           a p-type substrate of forming a base for said semiconductor structure;  
4           a first N<sup>+</sup> region within said substrate for forming a drain of a first MOS transistor;  
5           a second N<sup>+</sup> region within said substrate for forming a source of the first MOS transistor;  
6           a third N<sup>+</sup> region within said substrate coupled to a gate of a second MOS transistor, wherein  
7           a P<sup>+</sup> region is disposed adjacent to the third N<sup>+</sup> region for surrounding said first MOS  
8           transistor with an additional pick-up diffusion to reduce a turn-on speed or a longer channel length  
9           to increase a drain-base breakdown voltage of said first MOS transistor.

1            9. The semiconductor structure of claim 8, wherein said P+ region is disposed adjacent to  
2 the third N+ region for surrounding said first MOS transistor with an additional pick-up diffusion to  
3 reduce a turn-on speed and a longer channel length to increase a drain-base breakdown voltage of  
4 said first MOS transistor.

1            10. The semiconductor structure of claim 8, further comprising:  
2 a pre-buffer circuit coupled to said gate of the first MOS transistor; and  
3 an output pad coupled to said first region of the first MOS transistor.

1            11. The semiconductor structure of claim 8, further comprising:  
2 a first n-channel region having a first channel length and disposed between said first and  
3 second regions of said first MOS transistor;  
4 a second n-channel region having a second channel length and disposed between said first and  
5 second regions,  
6 wherein said first channel length is greater than said second channel length to further reduce  
7 a turn-on speed or a higher breakdown voltage of said first MOS transistor.

1            12. A semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide  
2 semiconductor (MOS) integrated circuit comprising:  
3 a p-type substrate forming a base for said semiconductor structure;  
4 a pair of first N+ regions within said substrate for defining a first n-channel region for a first  
5 MOS transistor; and

6 a pair of second N+ regions within said substrate for defining a second n-channel region for  
7 a second MOS transistor, wherein  
8 the channel length of said first channel is greater than the channel length of said second  
9 channel.

1 13. The semiconductor structure of claim 12, further comprising:  
2 a pre-buffer circuit coupled to said first channel region; and  
3 an output pad coupled to one of said pair of first N+ regions and one of said pair of second  
4 N+ regions.

1 14. The semiconductor structure of claim 12, further comprising a third region of the first  
2 conductivity type adjacent to one of said second N+ regions for surrounding said MOS transistor with  
3 an additional pick-up diffusion to further restrain the turn-on speed of said first MOS transistor.

1 15. A semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide  
2 semiconductor (MOS) integrated circuit, said semiconductor structure connected between an input  
3 pad and an internal circuit of said integrated circuit and comprising:

4 a substrate of a first conductivity type forming a base for said semiconductor structure;  
5 a first channel of a second conductivity type formed between first regions of said second  
6 conductivity type within said substrate for a first MOS transistor; and  
7 a second channel of the second conductivity type formed between second regions of said  
8 second conductivity type within said substrate for a second MOS transistor, wherein

9 an additional pick-up diffusion region is disposed adjacent to said first regions of said second  
10 conductivity type to reduce a turn-on speed or increase a drain breakdown voltage of said first MOS  
11 transistor.

1 16. The semiconductor structure of claim 15, wherein the channel length of said first channel  
2 is greater than the channel length of said second channel.

1 17. A semiconductor structure for electrostatic discharge (ESD) protection of a high-voltage  
2 tolerant I/O cells with stacked NMOS or PMOS integrated circuit, said semiconductor structure  
3 connected between a pre-driver circuit and an input/output pad of said integrated circuit and  
4 comprising:

5 a substrate of a first conductivity type forming a base for said semiconductor structure;  
6 a first channel of a second conductivity type formed between first regions of said second  
7 conductivity type within said substrate for a first MOS transistor which is stacked on a third  
8 MOSFET of a second conductivity type; and

9 a second channel of the second conductivity type formed between second regions of said  
10 second conductivity type within said substrate for a second MOS transistor which is stacked on a  
11 fourth MOSFET of a second conductivity type, wherein

12 an additional pick-up diffusion region is disposed adjacent to said first regions of said second  
13 conductivity type to reduce a turn-on speed and/or a longer channel length to increase a drain-base  
14 breakdown voltage of said first MOS transistor.

1 18. The semiconductor structure of claim 17, wherein the channel length of said first channel  
2 is greater than the channel length of said second channel.

1 19. A semiconductor structure for electrostatic discharge (ESD) protection, comprising:  
2 at least one ESD protection device; and  
3 at least one guarded device which is turned-on by a turn-on restrain means, wherein the ESD  
4 protection device can be turned-on before the guarded device is turned-on.

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